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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,067	11/19/2003	Darren L. Anand	BUR920030161US1	1066

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GARDEN CITY, NY 11530

EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,067	ANAND ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2 and 15 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In this instant, claims 2 and 15 define the intended use of the circuit in claims 2 and 14, respectively, rather than to further limit the subject matter of the circuit of claims 1 and 14.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 14, the recitation of "a plurality of secondary phase lock circuits for synchronizing a plurality of internal clock signals to one of a plurality of selected phases of the external reference clock" of claim 1, "synchronizing a plurality of internal clock signals to a one of a plurality of a selected phases of the external reference clock" in claim 14, are indefinite because it is misdescriptive of the present invention. Synchronizing is a common term used in the art. A signal is synchronizing to an another signal means that two edges of the signals are coincident. Claim 1 calls for a plurality of secondary phase lock circuits (one upper secondary phase locking circuit and two lower secondary phase locking circuits) for synchronizing a plurality of internal clock signals (CLK PHASE TAPS having 64 delayed version signals of the reference clock CKL) to one of a plurality of selected phases of the external reference clock is inconsistent with the known meaning of synchronizing. The plurality of the internal signals can not be in synchronization with the reference clock because the internal signals are the delayed version of the reference clock. Figure 3 shows a circuit providing a multi-phase clock signals (DOCLK, PCLK and SDCLK). The multi-phase clock signals can be chosen from the set of 64 delayed version signals of the reference clock by using the three secondary phase locked circuits. Therefore, the plurality of internal clock signals can not be in synchronized with one of the phase of the reference clock. Clarification and correction are required.

In claims 3 and 16, the recitation of "a plurality of internal clocks" is indefinite because it is unclear as to if these internal clocks are the same or are additional clocks to the internal clock signals recited in claims 1, line 10 and claim 14, line 7. Clarification and correction are required.

Claims 2, 4-13, 15 and 17-26 are indefinite because of the technical deficiencies of claims 1 and 14.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5 and 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirata et al. (USP 6,794,912). Figure 9 shows a modular digital locked loop for generating a plurality of multiple phase clock signals comprising a single core frequency locked circuit (210 of figure 9 or 310 of figure 10), comprising a delay element (320 of figure 10), a phase comparing circuit (313), a delay control (314, 315 of figure 10), for locking the single core frequency lock circuit to an external reference clock (REFCLK), a plurality of secondary phase locked circuits (230, 250, 270 delay circuits of figure 9 and detailed of one of the circuits is shown in figure 12), each receiving an output from the single core frequency lock circuit, for synchronizing a plurality of internal signals (CLKA, CLKB) to one of a plurality of selected phase of the external reference clock signals (CK1A, CK1B, CK2A, CK2B, CK3, CK3B are phase shifted version of the external clock) as called for in claims 1 and 14.

Regarding claims 2 and 15, the defined limitation is seemed to be an intended use of the DLL circuit, and the circuit of Hirata et al. is capable of synchronizing of an embedded DRAM system on a chip with on chip timing.

Regarding claims 3-4 and 16-17, the plurality of internal signals (CLKA, CLKB of figure 10) having the same frequency as the external reference and are phase displaced relative to each other.

Regarding claims 5 and 18, n is two.

Allowable Subject Matter

6. Claims 6-13 and 19-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Hirata et al. fails to teach or fairly suggest a clock select digital code for selecting a particular one of the generated plurality of internal clocks as called for in claims 6 and 19, latch receives the external reference clock as called for in claims 8 and 21.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited reference in the PTOL-1449 has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

11/2/2004